V3142 High-Speed Dual-Channel Digital Isolators

1. Key Features

- Signal Rate: DC to 150Mbps
- Wide Operating Supply Voltage: 2.5V to 5.5V
- Wide Operating Temperature Range: -40°C to 125°C
- No Start-Up Initialization Required
- Default Output High and Low Options
- High Electromagnetic Immunity
- High CMTI: ±100kV/µs (Typical)
- Low Power Consumption (Typical):
  - 1.5mA per Channel at 1Mbps with 5.0V Supply
  - 6.6mA per Channel at 100Mbps with 5.0V Supply
- Precise Timing (Typical)
  - 8ns Propagation Delay
  - 1ns Pulse Width Distortion
  - 2ns Propagation Delay Skew
  - 5ns Minimum Pulse Width
- Isolation Rating up to 5.0kVrms
- Isolation Barrier Life: >40 Years
- Schmitt Trigger Inputs
- RoHS-Compliant Packages
  - SOIC-8

2. Applications

- Industrial Automation Systems
- Motor Control
- Medical Electronics
- Isolated Switch Mode Supplies
- Solar Inverters
- Isolated ADC, DAC

3. Description

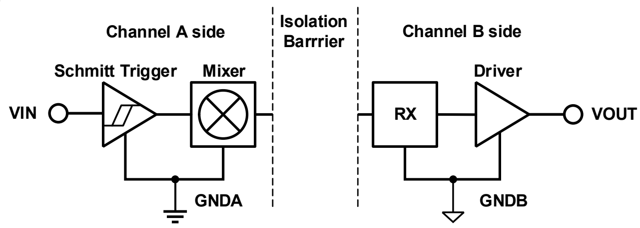
V3142 is high-performance dual-channel digital isolator with precise timing characteristics and low power consumption. It provides high electromagnetic immunity and low emissions, while isolating CMOS digital I/Os. V3142 has Schmitt trigger input for high noise immunity. Each isolation channel consists of a transmitter and a receiver separated by silicon dioxide (SiO_2) insulation barrier. The V3142 device has one forward and one reverse-direction channels. All devices have fail-safe mode option. If the input power or signal is lost, default output is high.

V3142 has high insulation capability to handle noise and surge on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. High CMTI ability promises the correct transmission of digital signal. V3142 is available in 8-pin SOIC packages. All products have 3.75kVrms isolation rating.

Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
V3142	SOIC8 (S)	4.90 mm ×3.90 mm

Simplified Channel Structure



Channel A side and B side are separated by isolation capacitors. GNDA and GNDB are the isolated ground for signals and supplies of A side and B side respectively.

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4. Revision History

Version 1.0: Initial release.

Version 1.1: Update Ordering Guide.

5. PIN Descriptions and Functions

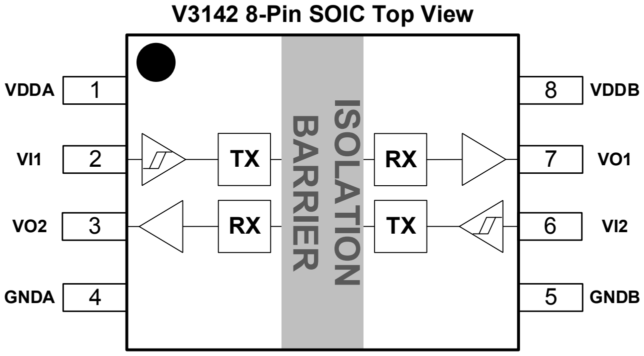


Figure 5-1 8-Pin SOIC Package Top View

Table 5-1 8-Pin SOIC Package Pin Description and Functions

Name	SOIC-8 Pin#	Type	Description
VDDA	1	Supply	Side A Power Supply
VI1	2	Digital I/O	Side A Digital Input for V3142
VO2	3	Digital I/O	Side A Digital Output for V3142
GNDA	4	Ground	Side A Ground
GNDB	5	Ground	Side B Ground
VI2	6	Digital I/O	Side B Digital Input for V3142
VO1	7	Digital I/O	Side B Digital Output for V3142
VDDB	8	Supply	Side B Power Supply

6. Specifications

6.1. Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Supply Voltage[2]	-0.5	6.0	V
V_{in}	Voltage at Ax, Bx, ENx	-0.5	V_{DDA}+0.5[3]	V
I_O	Output Current	-20	20	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

NOTE:
1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 6 V.

6.2. ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

NOTE:
1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3. Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{DDA}, V_{DDB}	Supply Voltage		2.375	3.3	5.5	V
$V_{DD\ (UVLO+)}$	VDD Under voltage Threshold When Supply Voltage is Rising		1.95	2.24	2.375	V
$V_{DD\ (UVLO-)}$	VDD Under voltage Threshold When Supply Voltage is Falling		1.88	2.10	2.325	V
$V_{HYS\ (UVLO)}$	VDD Under voltage Threshold Hysteresis		70	140	250	mV
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO} = 3.3V	-2			
		V_{DDO} = 2.5V	-1			
I_{OL}	Low-level Output Current	V_{DDO} = 5V			4	mA
		V_{DDO} = 3.3V			2	
		V_{DDO} = 2.5V			1	
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		150	Mbps
T_A	Ambient Temperature		-40	27	125	°C

NOTE:
1. V_{DDO}=Output-side V_{DD}

6.4. Thermal Information

THERMAL METRIC		S (SOIC) 8 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	54.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.7	°C/W

ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.7	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	°C/W

6.5. Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V3142						
P_D	Maximum Power Dissipation	$V_{DDA} = V_{DDB}$ = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave			120	mW
P_{DA}	Maximum Power Dissipation on Side-A				60	mW
P_{DB}	Maximum Power Dissipation on Side-B				60	mW
P_{DA}	Maximum Power Dissipation on Side-A				60	mW
P_{DB}	Maximum Power Dissipation on Side-B				60	mW

6.6. Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE		UNIT
			W/G	S	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	14	14	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-III	
		Rated mains voltage ≤400 V_{RMS}	I-IV	I-III	
		Rated mains voltage ≤600 V_{RMS}	I-III	n/a	
DIN V VDE V 0884-11:2017-01[2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	637	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	450	V_{RMS}
		DC voltage	1414	637	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7070	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	6250	5000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After Input / Output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b1, At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^9$	$>10^9$	
	Pollution degree		2	2	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5.0	3.75	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

6.7. Safety-Related Certifications

VDE(Pending)	CSA(Pending)	UL(Pending)	CQC(Pending)	TUV(Pending)
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013
File	File	File	File	File

6.8. Electrical Characteristics

6.8.1. $V_{DDA} = V_{DDB} = 5\ V \pm 10\%$, $T_A = -40$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; *See Figure 7-1*	V_{DDO}-0.4	4.8		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; *See Figure 7-1*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at Ax or Bx or ENx			4	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-4			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	$V_I = V_{DDI}$[1] or 0 V, V_{CM} = 1200 V; *See Figure 7-3*	75	100		kV/μS
C_I	Input Capacitance[3]	$V_I = V_{DD}/ 2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, V_{DD} = 5 V		2		pF

NOTE:

1. V_{DDI} = Input-side V_{DD}
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω ±40%.
3. Measured from pin to Ground.

6.8.2. $V_{DDA} = V_{DDB} = 3.3\ V \pm 10\%$, $T_A = -40$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; *See Figure 7-1*	V_{DDO}-0.4	3.1		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; *See Figure 7-1*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DDA}$ at Ax or Bx or ENx			4	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-4			μA
Z_O	Output Impedance			50		Ω
CMTI	Common-mode Transient Immunity	$V_I = V_{DDI}$ or 0 V, V_{CM} = 1200 V; *See Figure 7-3*	75	100		kV/μs
C_I	Input Capacitance	$V_I = V_{DD}/ 2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, V_{DD} = 3.3 V		2		pF

6.8.3. V_{DDA} = V_{DDB} = 2.5 V ±5%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; *See Figure 7-1*	V_{DDO}-0.4	2.3		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; *See Figure 7-1*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at Ax or Bx or ENx			4	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-4			µA
Z_O	Output Impedance			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI} or 0 V, V_{CM} = 1200 V; *See Figure 7-3*	75	100		kV/µS
C_I	Input Capacitance	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 2.5 V		2		pF

6.9. Supply Current Characteristics

6.9.1. V_{DDA} = V_{DDB} = 5 V ±10%, T_A = -40 to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
V3142							
Supply Current – DC Signal	V_{IN} = 0V (L); V_{IN} = V_{DDI} (H)		I_{DDA}		1.3	2.0	mA
			I_{DDB}		1.3	2.0	
	V_{IN} =V_{DDI} (L); V_{IN} = 0V (H)		I_{DDA}		2.1	3.1	
			I_{DDB}		2.1	3.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.8	2.6	
			I_{DDB}		1.8	2.6	
		10Mbps (5MHz)	I_{DDA}		2.2	3.3	
			I_{DDB}		2.2	3.3	
		100Mbps (50MHz)	I_{DDA}		7.0	10.5	
			I_{DDB}		7.0	10.5	

6.9.2. V_{DDA} = V_{DDB} = 3.3 V ±10%, T_A = -40 to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
V3142							
Supply Current – DC Signal	V_{IN} = 0V (L); V_{IN} = V_{DDI} (H)		I_{DDA}		1.3	2.0	mA
			I_{DDB}		1.3	2.0	
	V_{IN} =V_{DDI} (L); V_{IN} = 0V (H)		I_{DDA}		2.1	3.1	
			I_{DDB}		2.1	3.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.8	2.6	
			I_{DDB}		1.8	2.6	
		10Mbps (5MHz)	I_{DDA}		2.1	3.2	
			I_{DDB}		2.1	3.2	
		100Mbps (50MHz)	I_{DDA}		5.5	8.2	
			I_{DDB}		5.5	8.2	

6.9.3. V_{DDA} = V_{DDB} = 2.5 V ±5%, T_A = -40 to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
V3142							
Supply Current – DC Signal	V_{IN} = 0V (L); V_{IN} = V_{DDI} (H)		I_{DDA}		1.3	2.0	mA
			I_{DDB}		1.3	2.0	
	V_{IN} =V_{DDI} (L); V_{IN} = 0V (H)		I_{DDA}		2.1	3.1	
			I_{DDB}		2.1	3.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each	1Mbps (500kHz)	I_{DDA}		1.8	2.6	
			I_{DDB}		1.8	2.6	
		10Mbps	I_{DDA}		2.0	3.0	

	Channel	(5MHz)	I_{DDB}	2.0	3.0	
		100Mbps	I_{DDA}	4.5	6.7	
		(50MHz)	I_{DDB}	4.5	6.7	

6.10. Timing Characteristics

6.10.1. V_{DDA} = V_{DDB} = 5 V ±10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 7-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]			2.0	4.5	ns
t_r	Output Signal Rise Time	*See Figure 7-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 7-1*		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	*See Figure 7-2*		8	12	ns
t_{SU}	Start-up Time			15	40	µs

NOTE:
1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

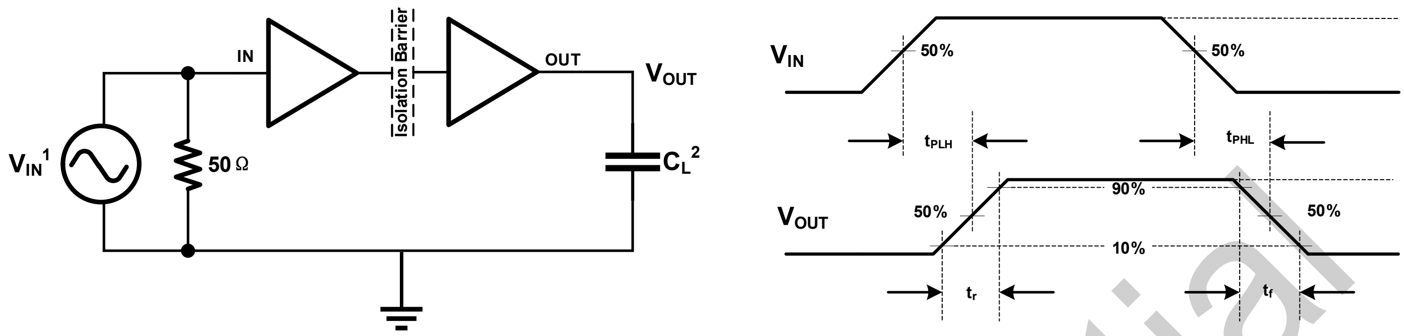
6.10.2. V_{DDA} = V_{DDB} = 3.3 V ±10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 7-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time			2.0	4.5	ns
t_r	Output Signal Rise Time	*See Figure 7-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 7-1*		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	*See Figure 7-2*		8	12	ns
t_{SU}	Start-up Time			15	40	µs

6.10.3. V_{DDA} = V_{DDB} = 2.5 V ±5%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 7-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	5.0	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time			2.0	5.0	ns
t_r	Output Signal Rise Time	*See Figure 7-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 7-1*		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	*See Figure 7-2*		8	12	ns
t_{SU}	Start-up Time			15	40	µs

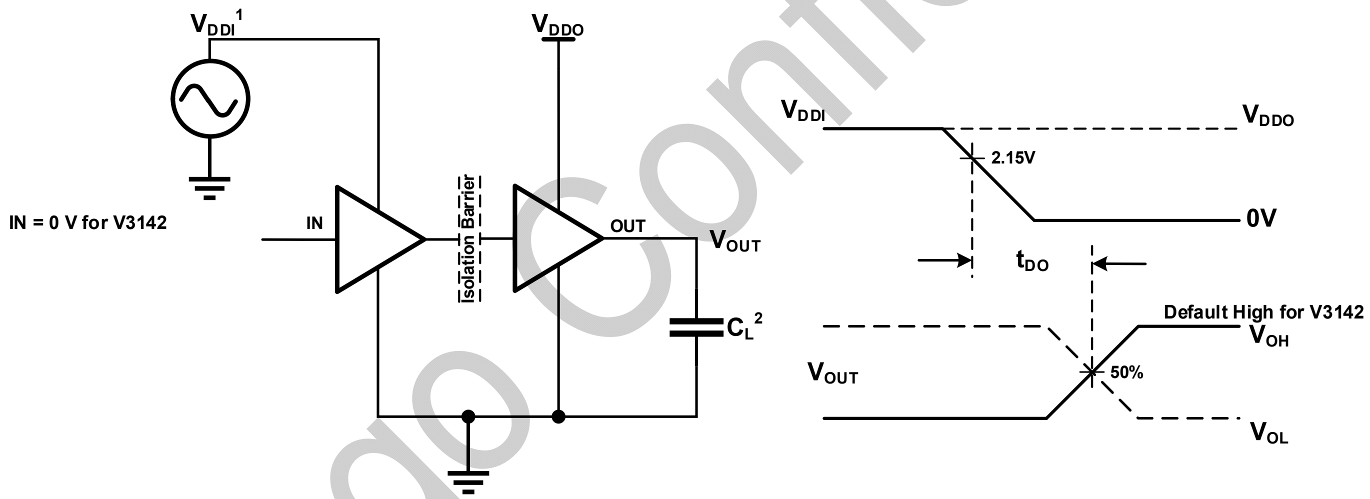
7. Parameter Measurement Information



NOTE:

1. A square wave generator generate the V_{IN} input signal with the following constraints: waveform frequency ≤100kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns. Since the waveform generator has an output impedance of Z_{out} = 50Ω, the 50Ω resistor in the figure is used for matching. There is no need in the actual application.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

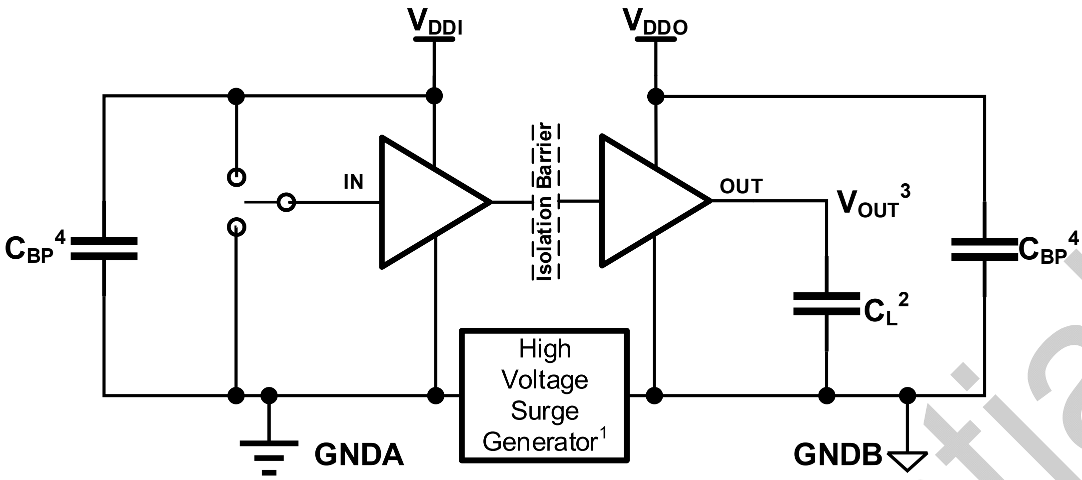
Figure 7-1 Timing Characteristics Test Circuit and Voltage Waveforms



NOTE:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should ramp over 2.15V but no higher than 5.5V.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 7-2 Default Output Delay Time Test Circuit and Voltage Waveforms



NOTE:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude and <10ns rise time and fall time to reach common-mode transient noise with > 100kV/µs slew rate.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges come.
4. C_{BP} is the 0.1 ~ 1uF bypass capacitance.

Figure 7-3 Common-Mode Transient Immunity Test Circuit

8. Detailed Description

8.1. Theory of Operation

V3142 use a simple ON-OFF keying (OOK) modulation scheme to transmit signal across the SiO_2 isolation capacitors that provide a robust insulation between two different voltage domain and act as a high frequency signal path between the input and the output. The transmitter (TX) modulates the input signal onto the carrier frequency, that is, TX delivers high frequency signal across the isolation barrier in one input state and delivers no signal across the barrier in the other input state. Then the receiver rebuilds the input signal according to the detected in-band energy. This simple architecture offers a robust isolated data path and requires no special considerations or initialization at start-up. The capacitor-based signal path is fully differential to maximize noise immunity, which is also known as common-mode transient immunity. Advanced circuitry techniques are applied for better EMI introduced by the carrier signal and IO switching. The capacitively-coupled architecture provides much higher electromagnetic immunity compared to the inductively-coupled one. And OOK modulation scheme eliminates the missing-pulse error that occurs in the pulse modulation method. A simplified functional block diagram and conceptual operation waveforms of a single channel is shown in Figure 9-1 and Figure 9-2.

8.2. Functional Block Diagram

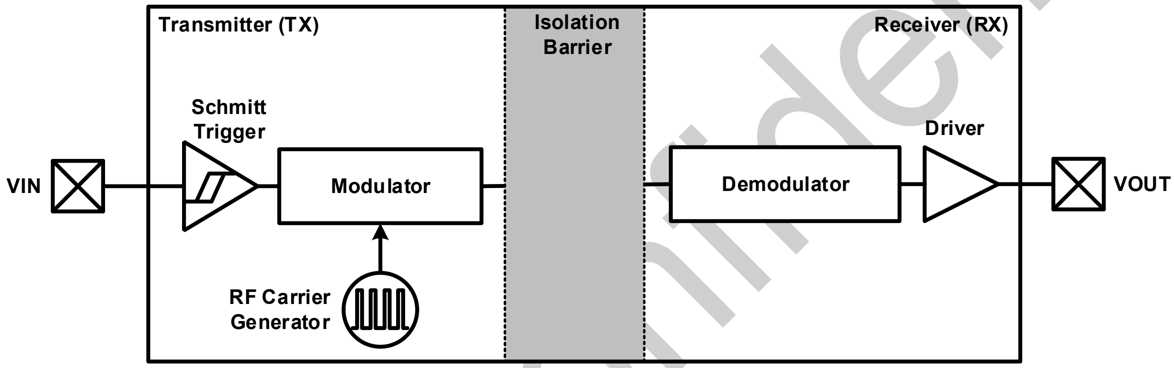


Figure 8-1 Functional Block Diagram of a Single Channel

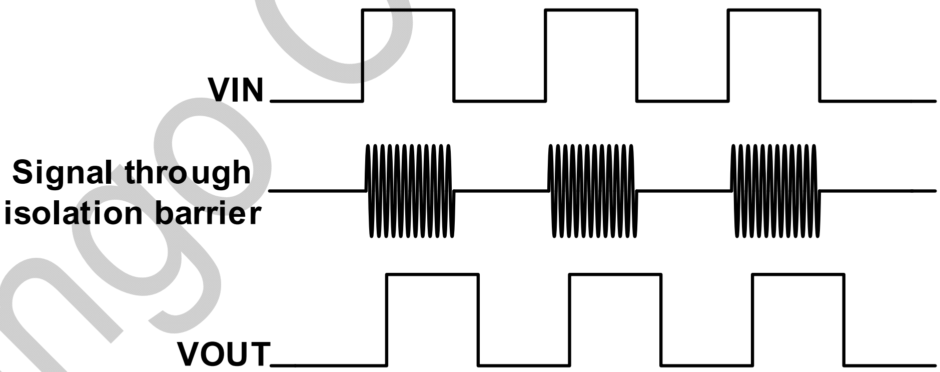


Figure 8-2 Conceptual Operation Waveforms of a Single Channel

8.3. Device Operation Modes

Table 8-1 Operation Mode Table[1]

V_{DDI}	V_{DDO}	INPUT(Ax/Bx)[2]	OUTPUT (Ax/Bx)	OPERATION
PU	PU	H	H	Normal operation mode: A channel's output follows the input state
		L	L	
		Open	Default	Default output fail-safe mode: If a channel's input is left open, its output goes to the default value (High for V3142).
PD	PU	X	Default	Default output fail-safe mode: If the input side VDD is unpowered, the outputs go in to the default output fail-safe mode (High for V3142)
X	PD	X	Undetermined	If the output side VDD is unpowered, the outputs' states are undetermined.[3]

NOTE:

1. V_{DDI} = Input-side V_{DD}; V_{DDO} = Output-side V_{DD}; PU = Powered up (VCC ≥ 2.375 V); PD = Powered down (VCC ≤2.25 V); X = Irrelevant; H= High level; L = Low level.
2. A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.
3. The outputs are in undetermined state when 2.25V< V_{DDI}, V_{DDO}< 2.375 V.

9. Application and Implementation

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, V3142 CMOS digital isolator needs only two external VDD bypass capacitors (0.1μF to 1μF) to operate. Its TTL level compatible input terminals draw only micro amps of leakage current, allowing them to be driven without external buffering circuits. The output terminals have a characteristic impedance of 50Ω (rail-to-rail swing) and are available in both forward and reverse channel configurations. Figure 10-1 shows the typical application. And the circuit of Figure 10-2 is typical for most applications of V3142 and is as easy to use as a standard logic gate.

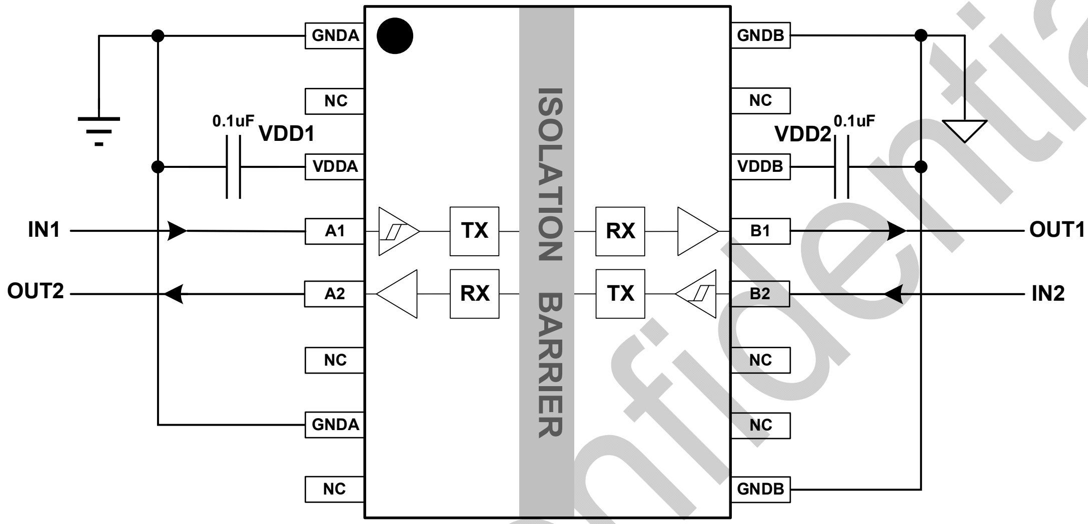


Figure 9-1 Typical Application Circuit

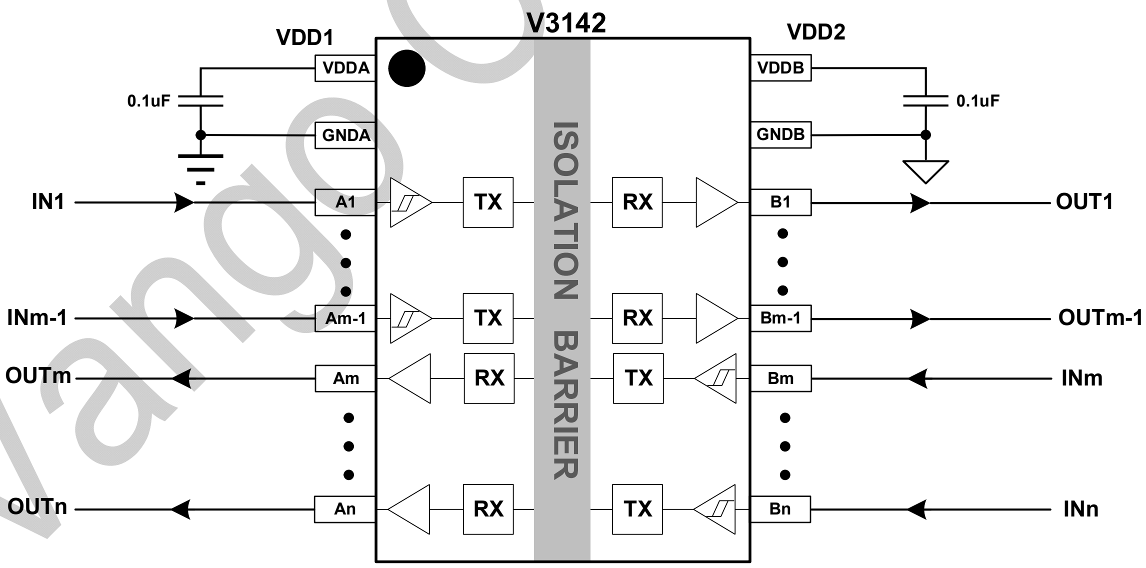
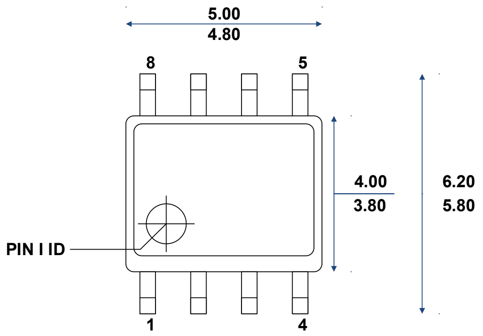


Figure 9-1 Digital Isolator Application Schematic

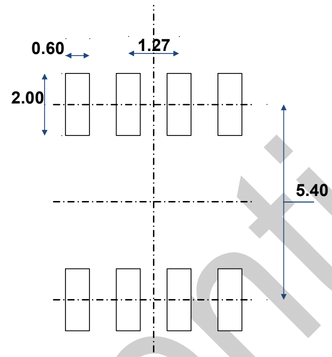
10. Package Information

10.1. 8-Pin SOIC Package Outline

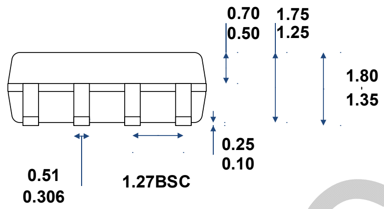
The figure below illustrates the package details and the recommended land pattern details for V3142 in an 8-pin narrow-body SOIC package. The values for the dimensions are shown in millimeters.



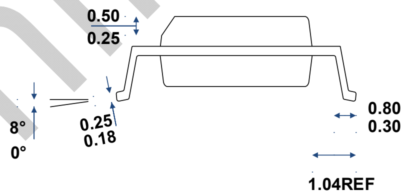
TOP VIEW



RECOMMENDED LAND PATTERN



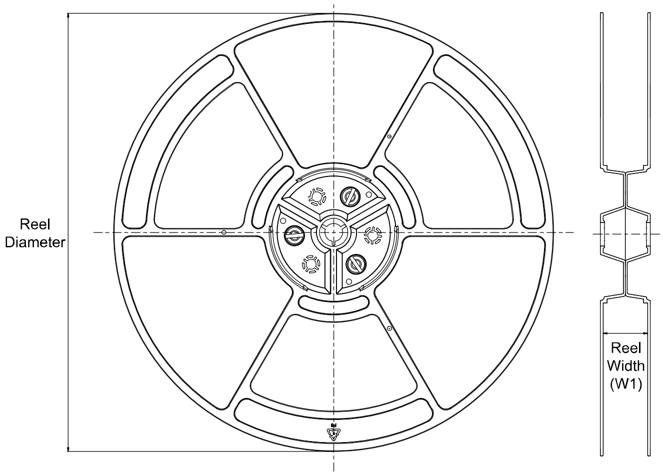
FRONT VIEW



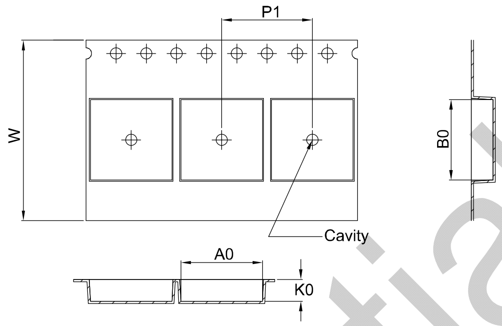
LEFT-SIDE VIEW

TAPE AND REEL INFORMATION

REEL DIMENSIONS

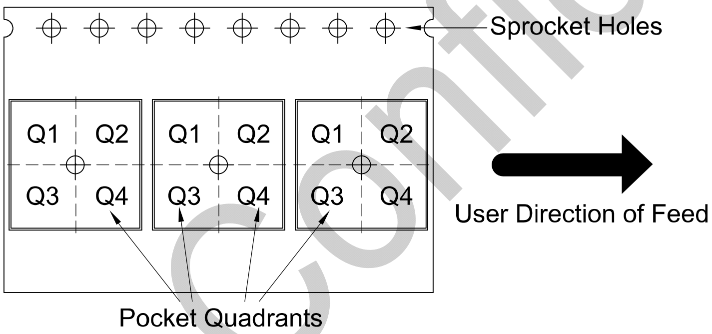


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
V3142/R	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1

11. Ordering Guide

Table 11-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating(kV)	Output Enable	Package
V3142	1	1	High	3.75	No	SOIC-8